

FIG. 1

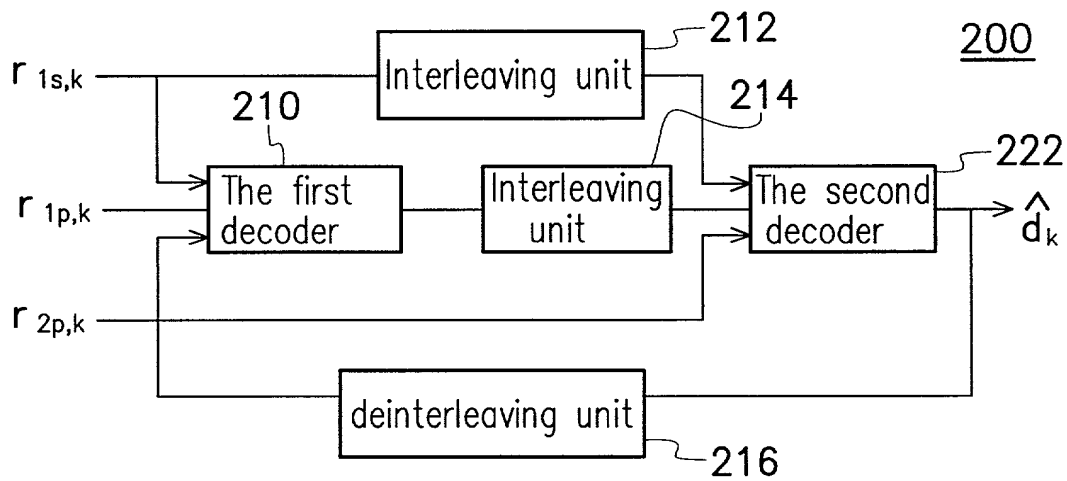


FIG. 2

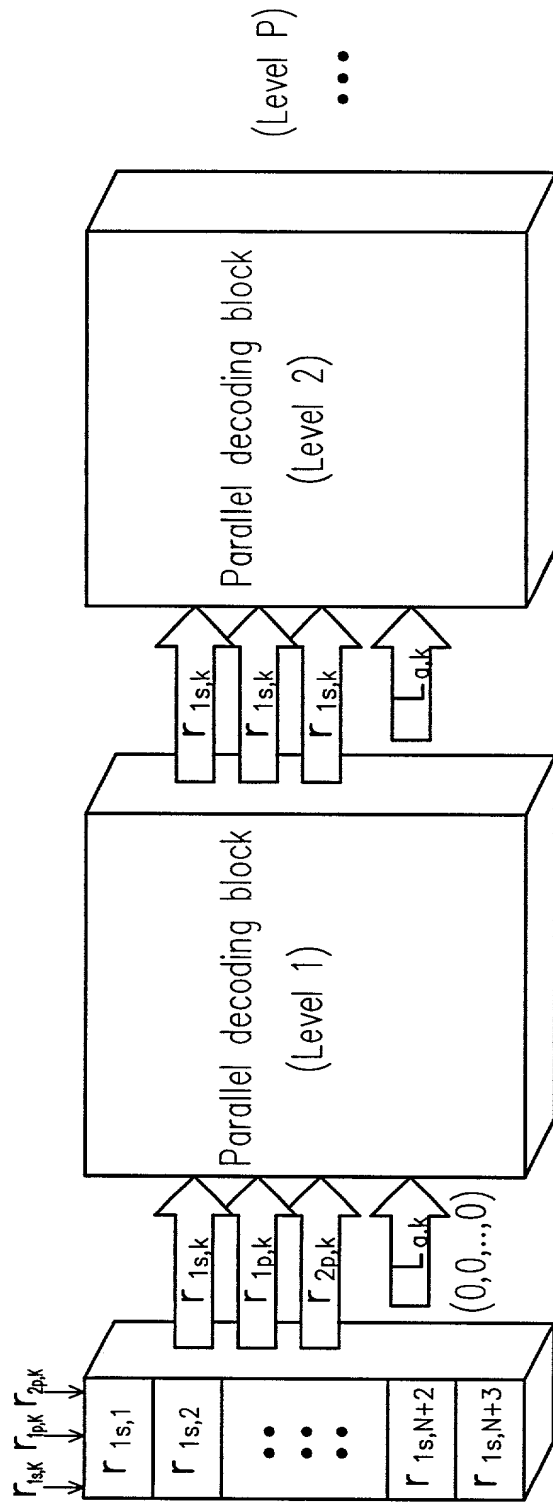


FIG. 3

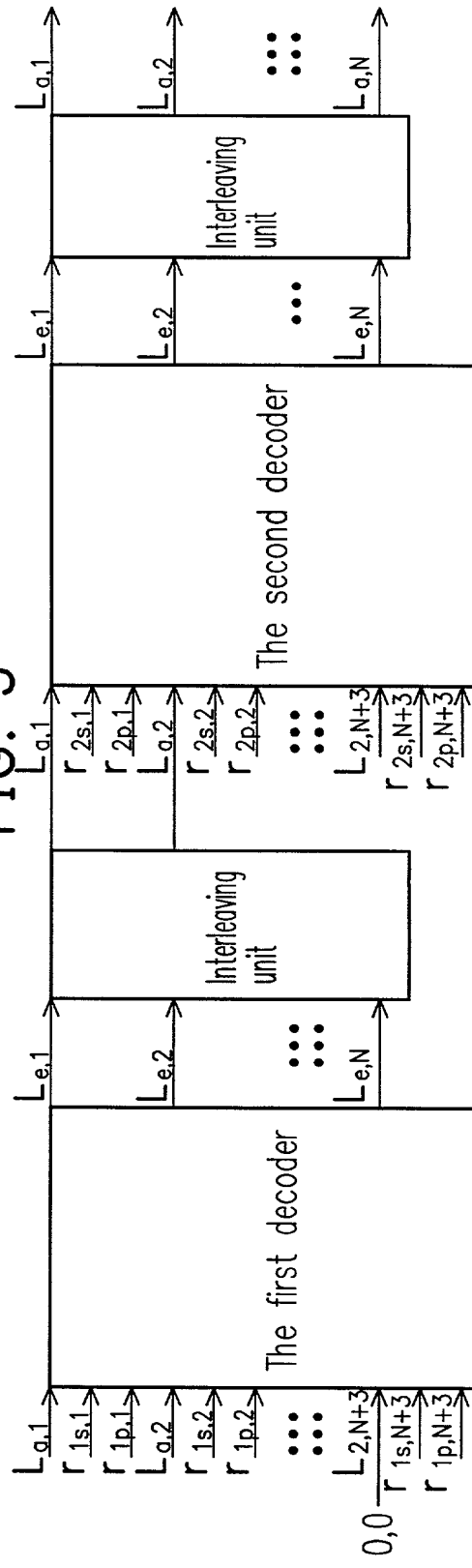
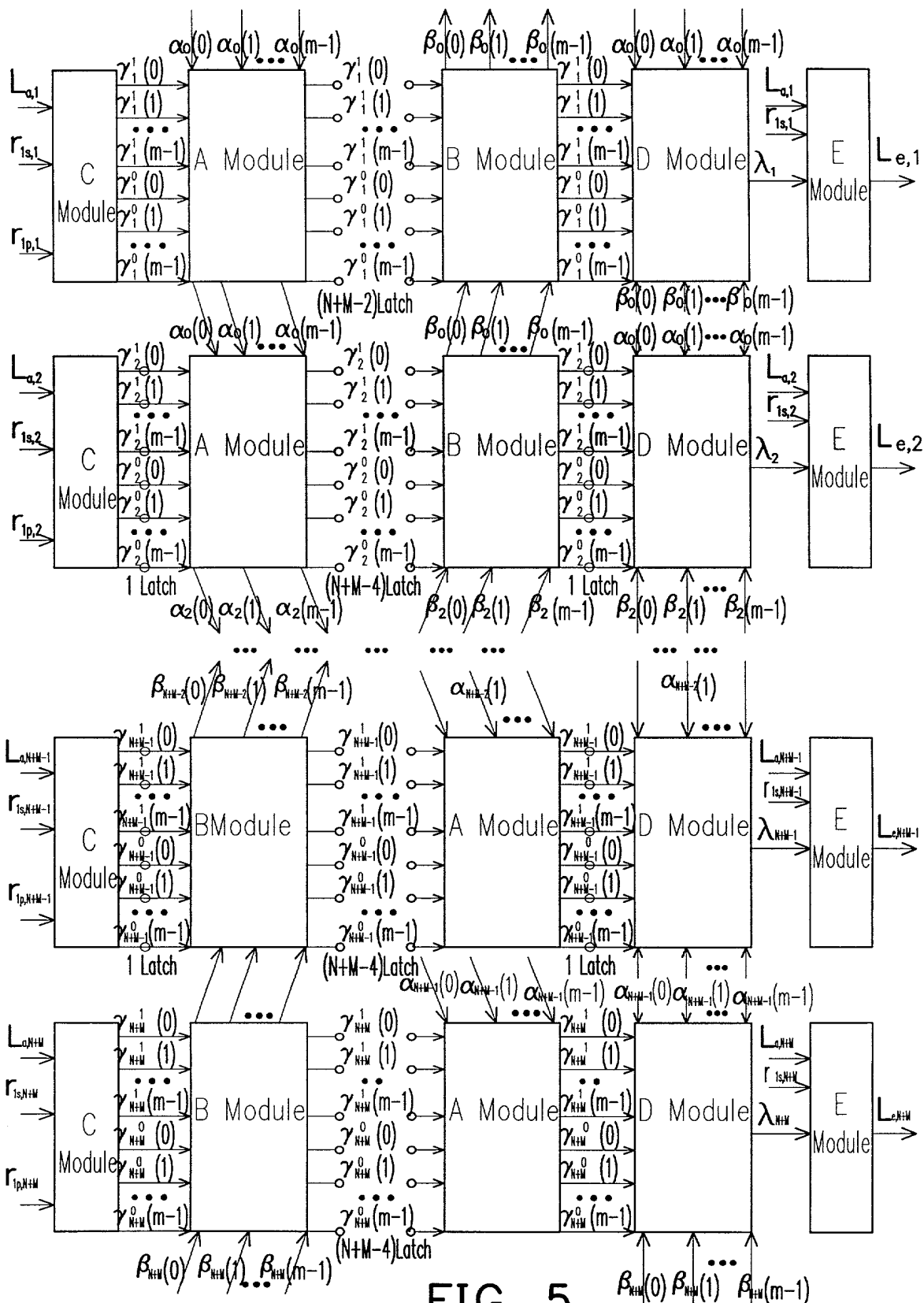


FIG. 4





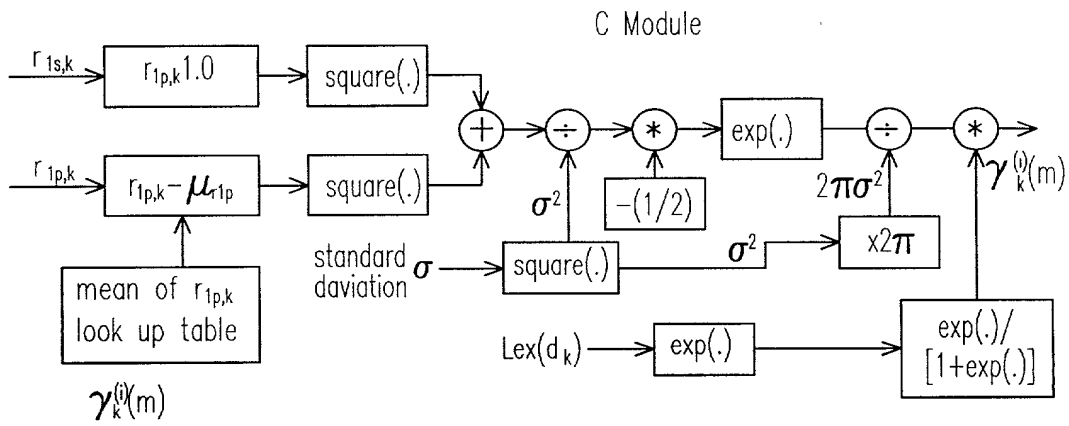


FIG. 7

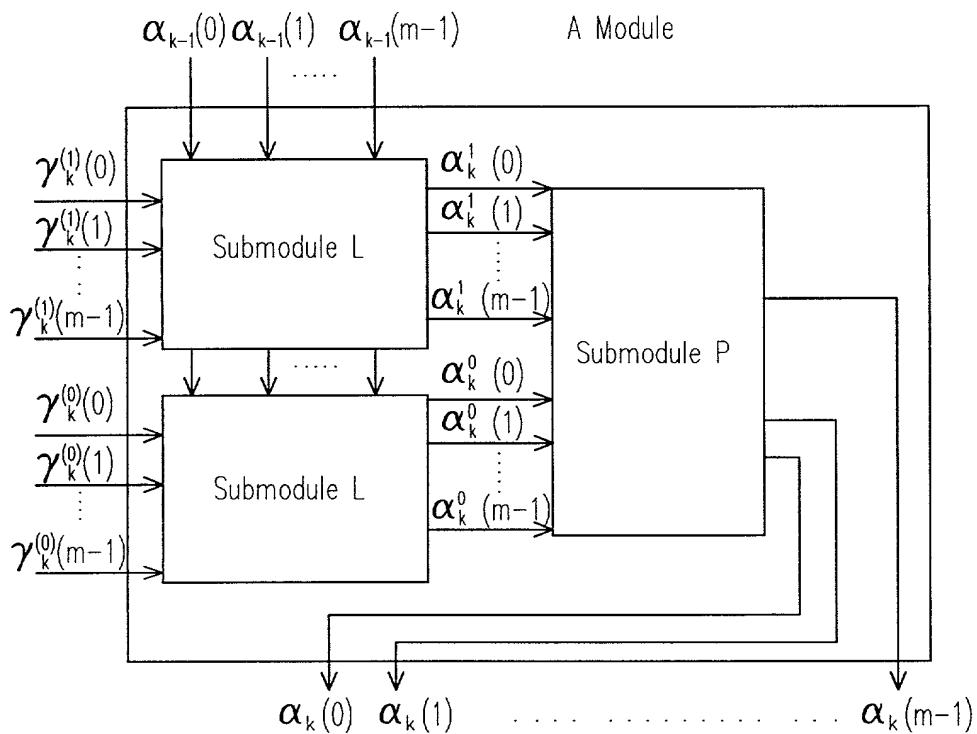


FIG. 8

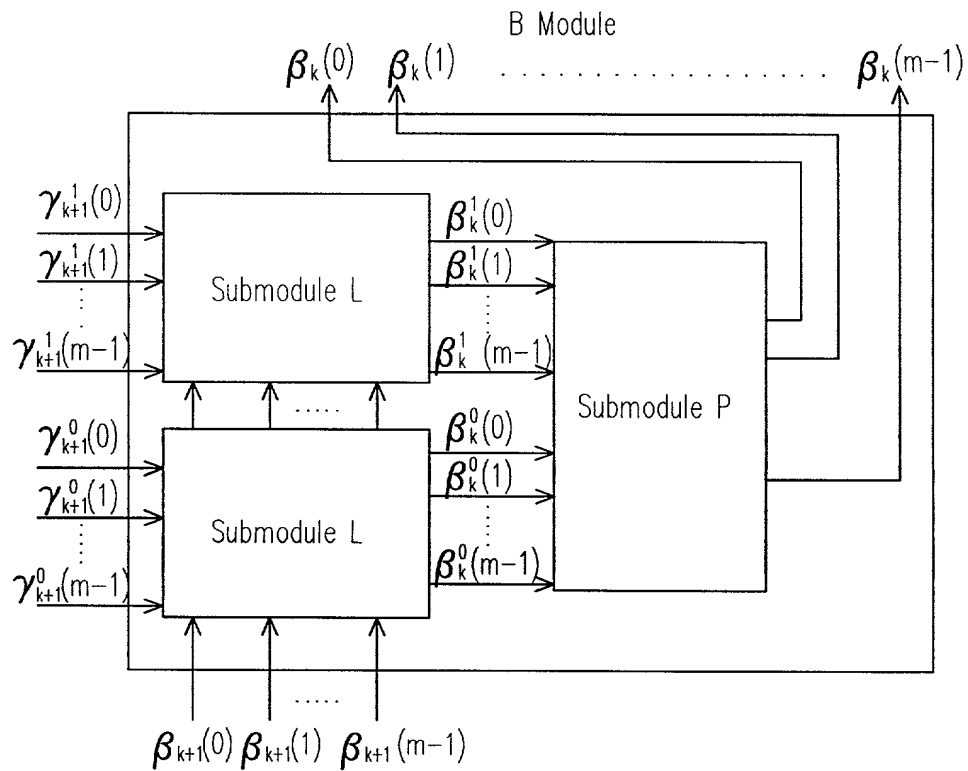


FIG. 9

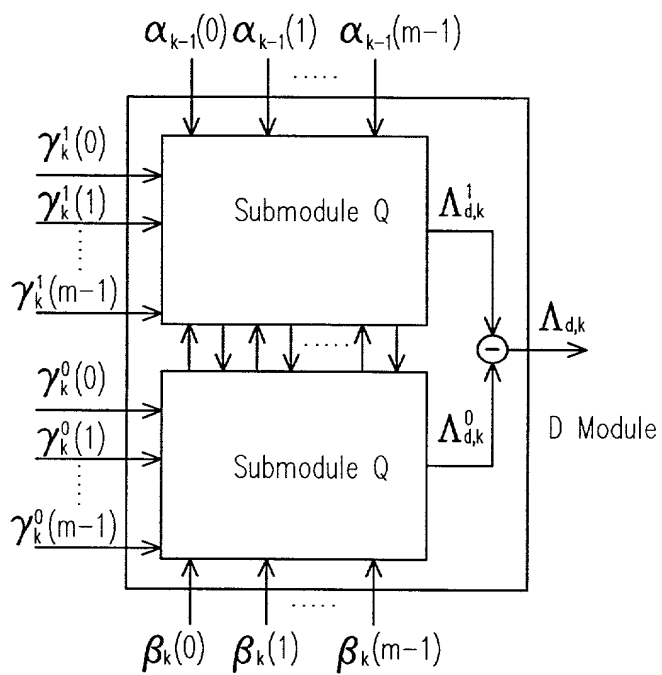


FIG. 10

FIG. 11 is a schematic diagram of a Submodule L structure. The diagram shows a multi-phase inverter circuit with  $m$  phases. The input is a reference voltage  $V_{ref}$ . The output is a set of  $m$  phase currents  $I_{y,1}, I_{y,2}, \dots, I_{y,m}$ . The circuit consists of  $m$  legs, each with two transistors (IGBTs) and an anti-parallel diode. The output of each leg is connected to a common bus. The output current of each leg is labeled  $I_{x,1}, I_{x,2}, \dots, I_{x,m}$ . The output voltage of each leg is labeled  $I_{y,1}, I_{y,2}, \dots, I_{y,m}$ . The output current of each leg is also labeled  $I_{1,1}, I_{1,2}, \dots, I_{1,m}, I_{2,1}, I_{2,2}, \dots, I_{2,m}, \dots, I_{m,1}, I_{m,2}, \dots, I_{m,m}$ .

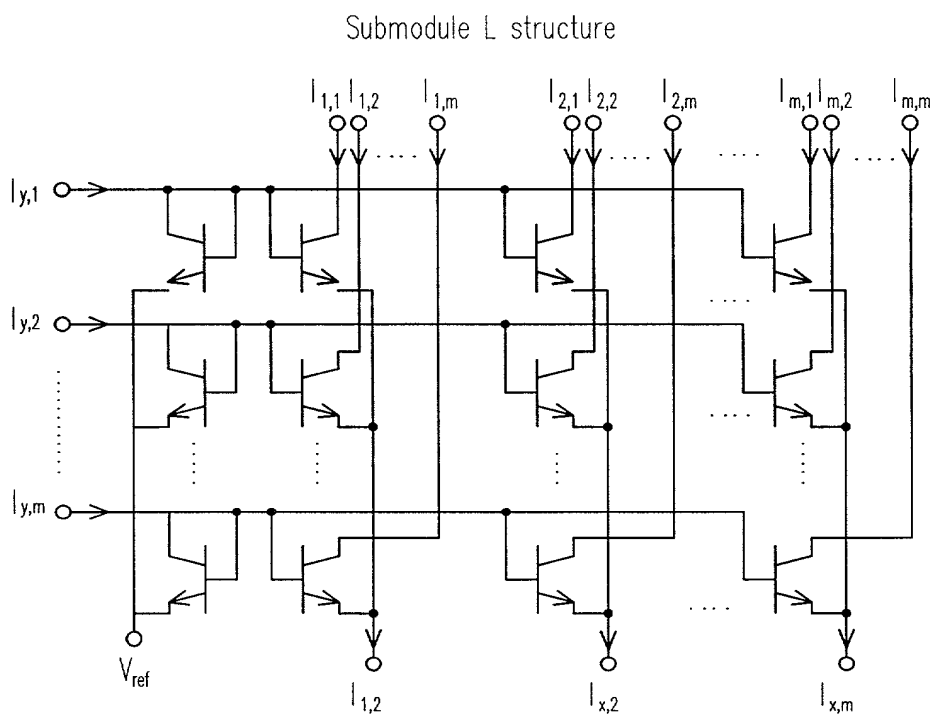


FIG. 11

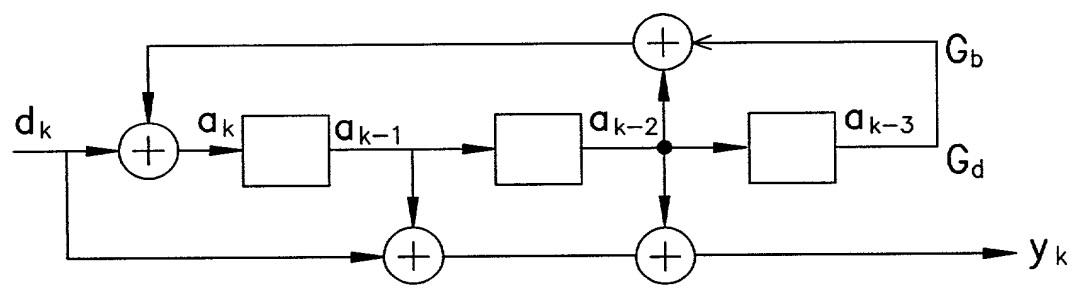


FIG. 12



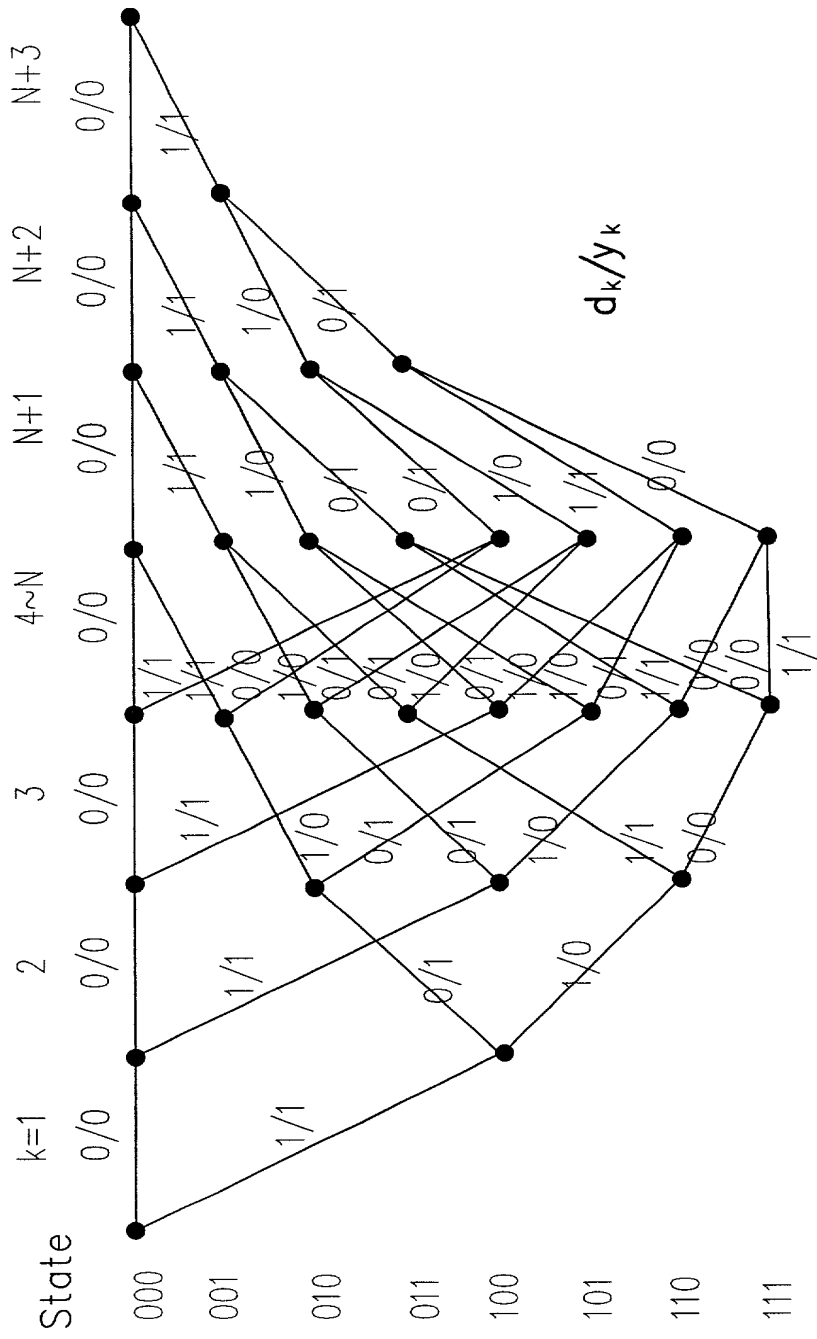


FIG. 13

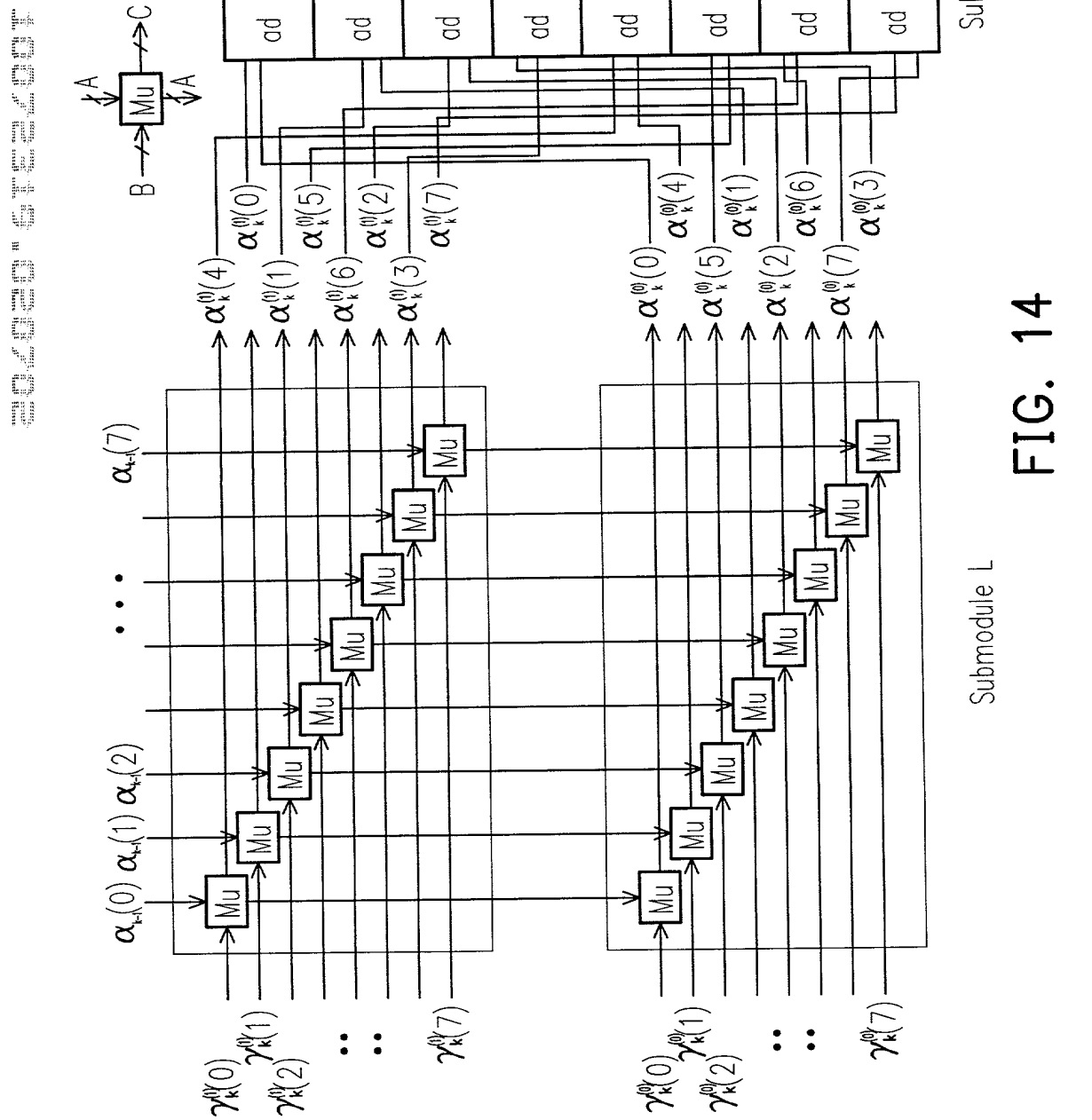
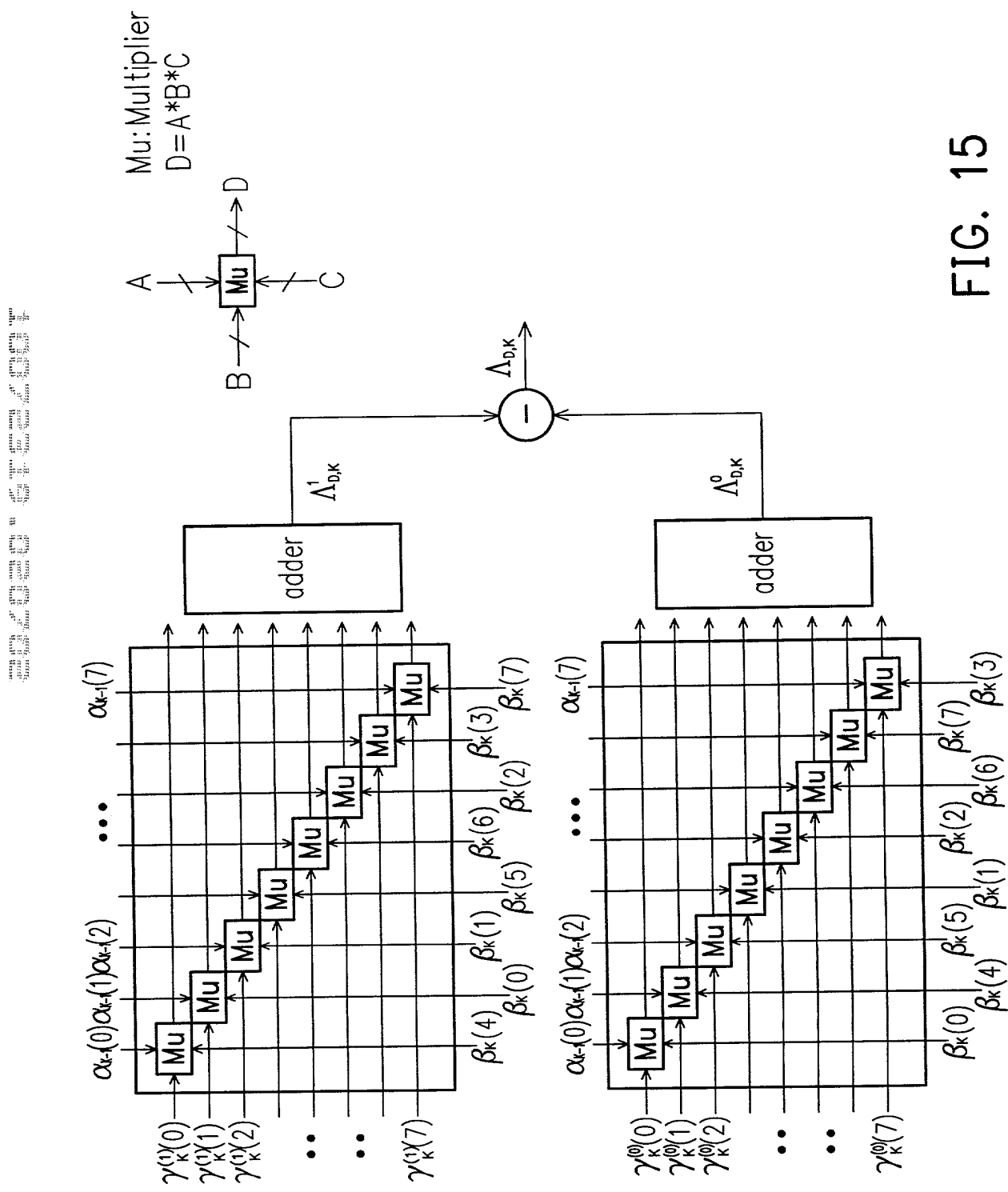


FIG. 14



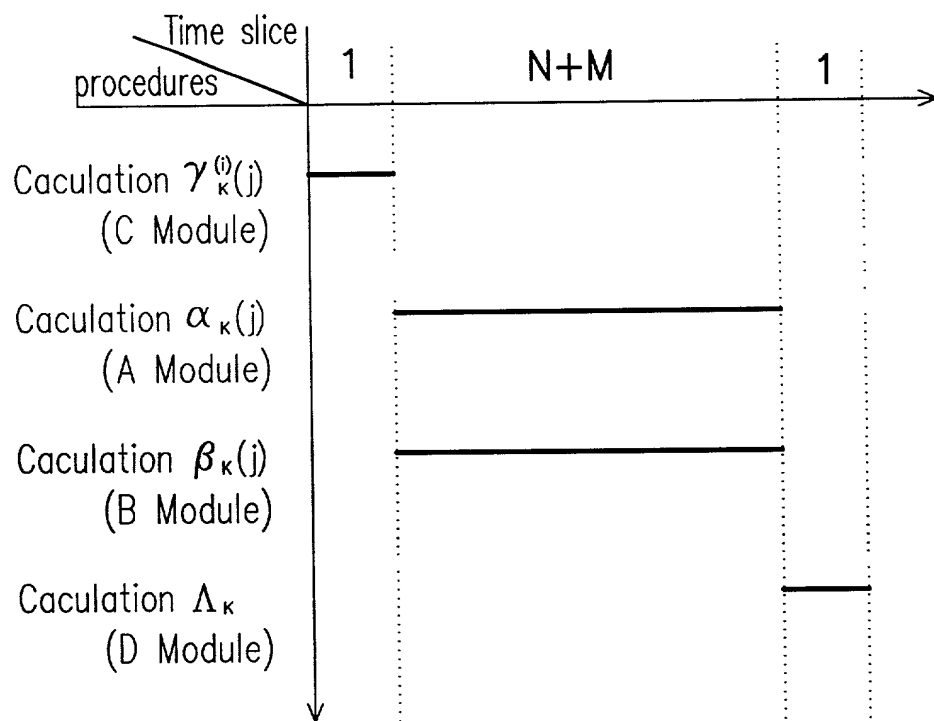


FIG. 16

